AMENDMENTS TO THE SPECIFICATION

Please replace the Abstract with the following paragraph of which an unmarked copy is attached:

-- Authentication circuits ~~2-3 to~~ 2-11 are provided between a debug I/F circuit ~~2-1~~ and a debug terminal. The authentication circuit transmits a transmission key ~~to~~ externally at the time of activation, and authenticates from a ~~received~~ reception signal and the transmission key, and enables ~~to~~ access ~~a~~ to the debug I/F. Thus, it It is possible to prevent a spurious access from the debug I/F by a third person by the authentication circuit. --.

Please replace the paragraph at p. 3, ls. 23-27, with the following:

-- It is yet another object of the present invention to provide an IC, an electronic device, a debug method, and a debugger for preventing the engineering of the authentication logic between the debug I/F circuit in the ~~LSIs~~ LSI and the external terminal. --.

Please replace the paragraph beginning at p. 4, l. 25, and ending at p. 5, l. 3, with the following:

-- According to a third aspect of the present invention there is provided a debugging method comprising the steps of transmitting the a transmission key to externally when the debug I/F circuit is activated; and authenticating ~~the~~ from a reception signal received ~~from~~ externally and the transmission key to enable operation of the debug I/F circuit. --.

Please replace the paragraph at p. 6, ls. 10-19, with the following:

-- Furthermore, in the LSI according to the present invention, the authentication circuit forms an authentication key by encoding ~~that is encoded~~ the transmission key by a predetermined key, and compares the reception signal with the authentication key. In the debugging method according to the present invention, the authentication step has a step of forming the authentication key by encoding ~~that is encoded~~ the transmission key by the predetermined key, and of collating the reception signal with the authentication key. As encoded, the higher security is possible. --.

Please replace the paragraph beginning at p. 8, l. 25, and ending at p. 9, l. 3, with the following:

-- The LSI 2 has a debug I/F circuit 2-1, a CPU 2-2, a debug bus 4-1 for connecting an I/F circuit 2-1 and the CPU 2-2, and a peripheral circuit 2-12 connected to a CPU bus 4-2. The peripheral circuit 2-12 is different according to the use of the LSI ~~LSIs~~, for example, an electronic money funds transferring circuit that will be explained in Fig. 6 on. --.

Please replace the paragraph at p. 9, ls. 7-14, with the following:

-- A port ~~4-2~~ 2-3 receives write data of the CPU 2-2 from the CPU bus 4-2. A register 2-5 stores a debug I/F utilization transmission key formed by the CPU 2-2. A register 2-8 stores 10 an authentication key formed by the CPU 2-2. A transmission circuit 2-4 transmits the transmission key of the register 2-5 in synchronism with a clock supplied by the discrimination device 3. A shift register 2-6 receives a cryptographic key returned from the discrimination device [2] 3. --.

Please replace the paragraph at p. 11, ls. 3-10, with the following:

-- ④ In the LSI 2, the shift register 2-6 receives the returned the cryptographic key, and the agreement detection 5 circuit 2-9 compares it with the authentication key of the register 2-8, and only in the case where agreed, the agreement detection circuit 2-9 transmits the agreement detection to the, timer circuit 2-7. The timer circuit 2-7 waits for a constant time, and ~~canceled~~ cancels a reset signal to the internal 10 debug I/F 2-1 by the gate 2-11. --.

Please replace the paragraph beginning at p. 14, l. 25, and ending at p. 15, l. 1, with the following:

-- According to the embodiment of the present invention, the ~~description~~ discrimination device 3 adopts a method of encoding the received transmission key and ~~use~~ user ID by the a predetermined key, thereby preventing ~~that~~ the user ID is from being readily changed. --.

Please replace the paragraph at p. 15, ls. 9-18, with the following:

-- As shown in Fig. 6, the system LSI 2 is a card funds transferring LSI, and has a debit card funds transfer function 40, a credit card funds transfer function 41, an electronic money funds transfer function 42, and other service functions 43. For this reason, the LSI 2 is connected to an IC card reader/writer 30, a magnetic card reader 31, and a display and ~~key~~ ten-key pad 32. Furthermore, as occasion arises, the LSI 2 is connected to a receipt printer 33. These funds transfer functions 40 to 43 are realized by execution of the programs of the CPU 2-2 of the LSI 2. --.

Please replace the paragraph beginning at p. 15, l. 26, and ending at p. 16, l. 9, with the following:

-- The peripheral circuit 2-12 of the LSI 2 for the card funds transfer will be explained with reference to Fig. 7. The peripheral circuit 2-12 has a smart card controller 60, a MS (Magnetic stripe) control circuit 61, a LCD control circuit 62, a matrix KB control circuit 63, a memory controller 64, and serial I/O ports ~~69 to 72~~ 66 to 69. In Fig. 7, the above LSI 2 indicates a condition of being mounted on the target board 7, and for clarity of description of the LSI 2, only the CPU 2-2 65 and peripheral circuit 2-12 (60-64, ~~69-72~~ 66-69) are shown. Of course, the LSI 2 includes the debug I/F ~~2-1~~ and the authentication circuit. --.

Please replace the paragraph beginning at p. 16, ls. 10 – 20, with the following:

-- The smart card controller 60 reads/writes data of the IC card (called a smart card) via the IC card reader/writer 30. The MS control circuit controls the MS (magnetic stripe) reader 31. The LCD control circuit 62 controls a display of the LCD (liquid crystal display) 32-1. The matrix KB control circuit 63 recognizes an input of a ~~ten-key~~ ten-key pad 32-2. The memory controller 64 control an input/output into/from various memories (a ROM 65 70, a SRAM 66 71, a FLASH ~~67~~ 72, a SDRAM ~~68~~ 73) on the board 7. The serial ports ~~69 to 72~~ 66 to 68 are connected to drivers 73 to 75 of the ~~port~~ board 7 for inputting and outputting the serial data. These are each connected to the CPU bus ~~4~~-2. --.

Please replace the paragraph at p. 17, ls. 2-6, with the following:

-- An IC card 34-1 for customers ~~is exchanged~~ exchanges messages with a POS IC card 34-2 via the POS IFD 2, and the POS IC card 34-2 ~~is exchanged~~ exchanges messages with the IC

card 34-2 of the store controller 20 via an IFD 2 of the store controller 20, a terminal controller 11 of the store controller 20, a network 35, the POS terminal controller 11, and the POS IFD 2.

--.

Please replace the paragraph at p. 17, ls. 7-13, with the following:

-- For example, in the case where the electronic funds transfer is carried out by the IC card, a customer's data of the IC card 34-1 are stored in the POS IC card 34-2 via the POS IFD 2. Thereafter, the stored data of the POS IC card 34-2 are stored in the IC card 34-2 of the store controller 20 via the IFD 2 of the store controller 20, the terminal controller 11 of the store controller 20, the network 35, the POS terminal controller 11, and the POS IFD 2. --.